Austin Semiconductor, Inc.

Quad Line Receiver

AVAILABLE AS MILITARY SPECIFICATIONS

- Military Equivalent Screening - 883 1.2.2

GENERAL DESCRIPTION

The AS10515F16MIL is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the AS10515F16MIL with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

- P_D = 150mW Max/Pkg (No Load)
- t_{pd} = 2.0ns typ
- t_r, t_f = 2.0ns type (20% - 80%)

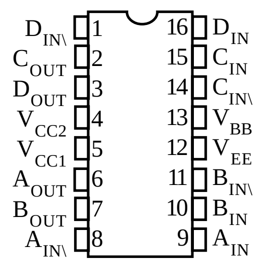
PIN ASSIGNMENTS

FUNCTION	FLATS	BURN-IN (CONDITION C)
V_{CC1}	5	GND
A_{OUT}	6	51 Ω to V_{TT}
B_{OUT}	7	51 Ω to V_{TT}
A_{IN}\	8	V_{BB}
A_{IN}	9	GND
B_{IN}	10	GND
B_{IN}\	11	V_{BB}
V_{EE}	12	V_{EE}
V_{BB}	13	V_{BB}
C_{IN}\	14	V_{BB}
C_{IN}	15	GND
D_{IN}	16	GND
D_{IN}\	1	V_{BB}
C_{OUT}	2	51 Ω to V_{TT}
D_{OUT}	3	51 Ω to V_{TT}
V_{CC2}	4	GND

PIN ASSIGNMENT

(Top View)

16-Pin FlatPack (F)



BURN-IN CONDITIONS:

V_{TT} = -2.0V MAX/ -2.2V MIN

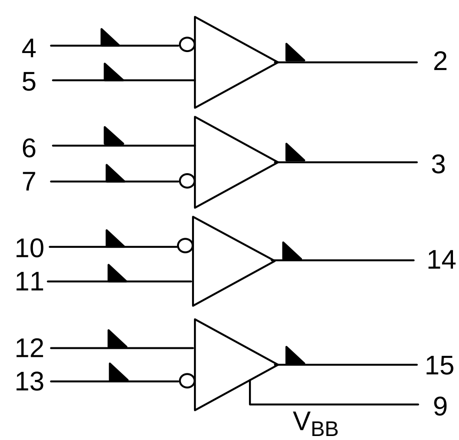
V_{EE} = -5.7V MAX/ -5.2V MIN

V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

NOTES

1. V_{BB} to be used to supply bias to the AS10515F16MIL only and bypassed (when used) with 0.01 µF to 0.1 µF capacitor.
2. When the input pin with the bubble goes positive, the output goes negative.

LOGIC DIAGRAM



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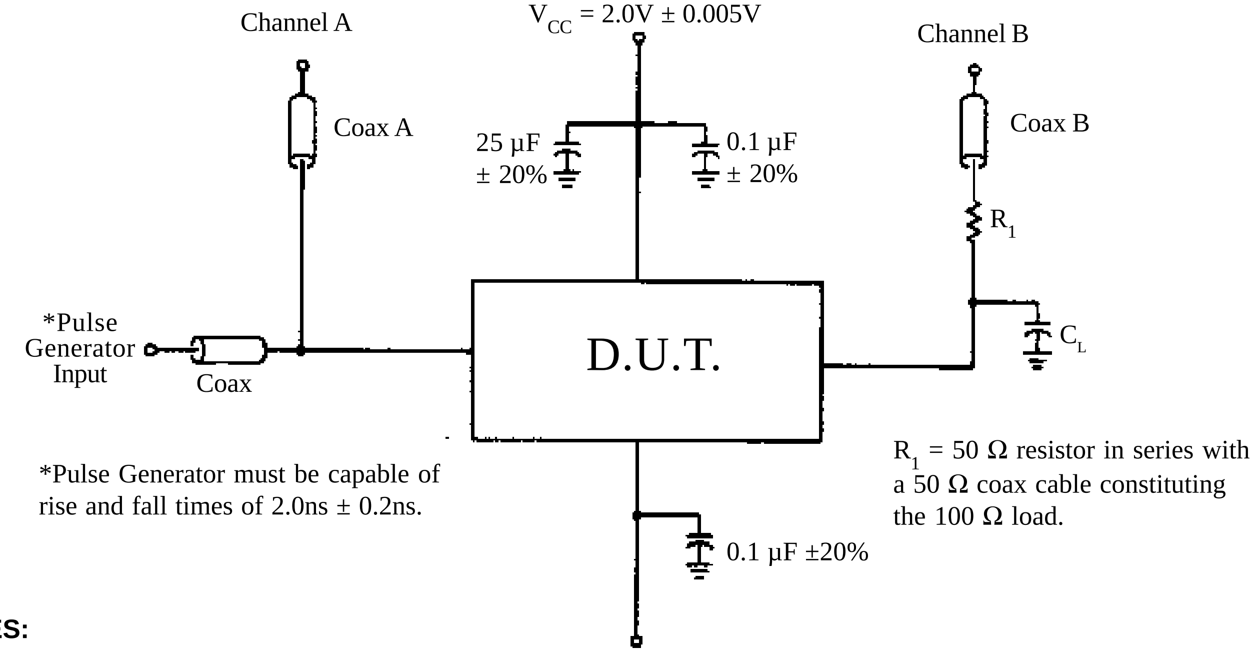

NOTES:

1. $t_r = t_f$ = 2.0ns ±0.2ns measured at (20% - 80%)
2. $P_W \geq$ 20ns
3. P_{RF} = 1.0 MHz
4. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
5. Unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.

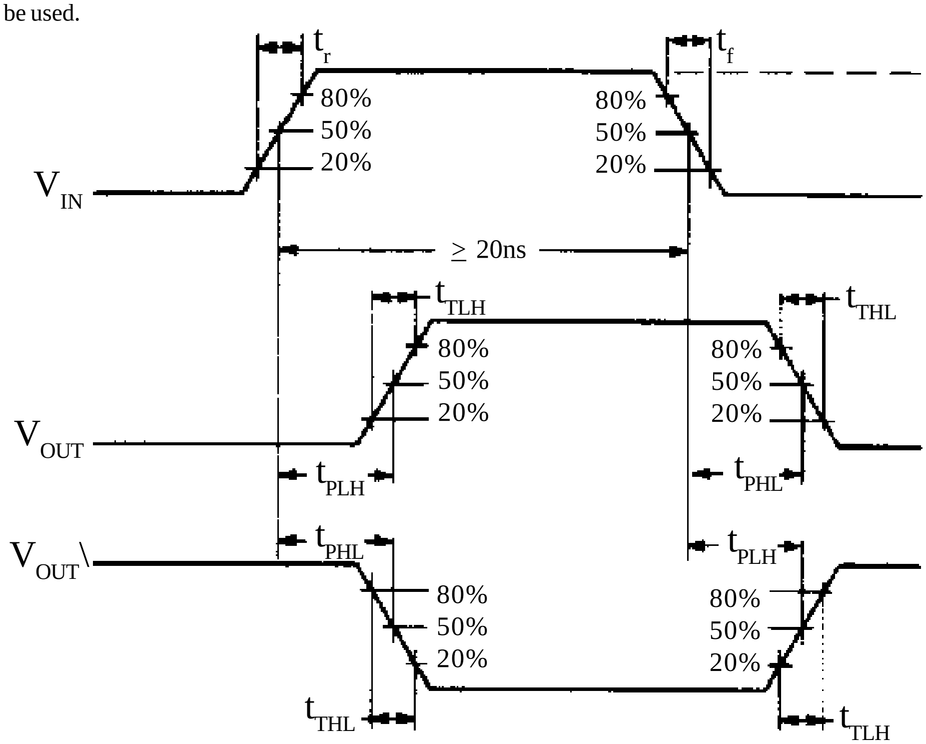

Figure 1. Switching Test Circuit and Waveforms

QUIESCENT LIMIT TABLE*

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE}	V_{CB}
T_A = 25°C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-3.2	-5.2	-5.2
T_A = 125°C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2
T_A = -55°C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2

SYMBOL	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW:							
	Functional Parameters:	+25°C Subgroup 1		+125°C Subgroup 2		-55°C Subgroup 3			Pinouts referenced are for F package, check Pin Assignments V_{CC} = 0V, Output Load = 100 Ω to -2.0V							
		MIN	MAX	MIN	MAX	MIN	MAX		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	***	P.U.T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	5, 6, 11, 12	4, 7, 10, 13			8	1, 16	4 - 7 11 - 13	2, 3 ,14, 15
V_{OL}	Low Output Voltage	-1.85	-1.62	-1.82	-1.545	-1.92	-1.655	V	4, 7, 10, 13	5, 6, 11, 12			8	1, 16	4 - 7 11 - 13	2, 3 ,14, 15
V_{OH1}	High Output Voltage	-0.95	-0.78	-0.845	-0.63	-1.10	-0.88	V			5, 6, 11, 12	4, 7, 10, 13	8	1, 16	4 - 7 11 - 13	2, 3 ,14, 15
V_{OL1}	Low Output Voltage	-1.85	-1.60	-1.82	-1.525	-1.92	-1.635	V			4, 7, 10, 13	5, 6, 11, 12	8	1, 16	4 - 7 11 - 13	2, 3 ,14, 15
**V_{BB}	Reference Voltage	-1.35	-1.23	-1.24	-1.12	-1.44	-1.32	V					8	1, 16	5, 6 11, 12	9
I_{EE}	Power Supply Current	-26		-29		-29		mA					8	1, 16	5, 6 11, 12	8
I_{IH}	Input Current High		95		165		165	µA	4 - 7 10 - 13				8	1, 16		4 - 7 10 - 13
I_{CBO}	Input Leakage Current	-1.0		-1.0		-1.5		µA					8	1, 16	4 - 7 10 - 13	4 - 7 10 - 13

** Connected to pin 9.

*** Measure voltage on pin 9 while it is connected to other pins.

QUIESCENT LIMIT TABLE*

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T_A = 125°C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2
T_A = -55°C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2

SYMBOL	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+25°C Subgroup 9		+125°C Subgroup 10		-55°C Subgroup 11			Pinouts referenced are for F package, check Pin Assignments V_{CC} = 2.0V, Output Load = 100 Ω to GND				
		MIN	MAX	MIN	MAX	MIN	MAX		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3 ,14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3 ,14, 15
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	4.0	1.0	3.5	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3 ,14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.90	1.0	4.0	1.0	3.5	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3 ,14, 15